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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
NGUYEN, TANH Q	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HUGO CHEUNG

Appeal 2009-010450
Application 10/650,403
Technology Center 2100

Before JOSEPH L. DIXON, LANCE LEONARD BARRY, and JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 15-17, 19, and 20.[1] We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

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[1] Although Appellant indicates that claim 18 is withdrawn from consideration (Br. 2), the Examiner cancelled that claim. Ans. 2.

STATEMENT OF THE CASE

Appellant's invention employs a buffering scheme for a serial peripheral interface that facilitates high data transmission rates between microprocessors, components, and other devices. *See generally* Spec. 1, 5-6. Claim 15 is illustrative with key disputed limitations emphasized:

15. A high performance buffering technique for use with a serial peripheral interface to facilitate high data rates, said buffering technique comprising the steps of

initializing a *single buffer* to act as transmitter and receiver by writing data to a data register;

performing a transmit buffering sequence to prepare for the transmitting of the data;

performing a *transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time*; and

performing a receive buffering sequence to prepare for the receipt of additional new data.

The Examiner relies on the following as evidence of unpatentability:

Thomsen	US 5,278,956	Jan. 11, 1994
Yasoshima	US 2002/0078317 A1	June 20, 2002 (filed Dec. 19, 2000)

THE REJECTION

The Examiner rejected claims 15-17, 19, and 20 under 35 U.S.C. § 103(a) as unpatentable over Thomsen and Yasoshima. Ans. 3-6.[2]

[2] Throughout this opinion, we refer to the Appeal Brief filed December 21, 2007 and the Examiner's Answer mailed March 13, 2009.

CONTENTIONS

Regarding representative claim 15, the Examiner finds that Thomsen discloses a buffering technique usable with a serial peripheral interface with every recited feature except for arranging the disclosed transmitter and receiver FIFO buffers in a single buffer, but cites Yasoshima for teaching arranging multiple FIFOs within a single buffer in concluding that the claim would have been obvious. Ans. 3-10.

Appellant argues that Yasoshima does not disclose a single buffer to facilitate transmitting and receiving substantially simultaneously, nor do the references teach how they can be combined to obtain a single buffer to perform a transmit and receive shifting sequence to facilitate transmitting data and receiving new data as claimed. Br. 5. The issues before us, then, are as follows:

ISSUES

1. Under § 103, has the Examiner erred in rejecting claim 15 by finding that Thomsen and Yasoshima collectively would have taught or suggested (1) initializing a single buffer to act as a transmitter and receiver by writing data to a data register, and (2) performing a transmit and receive shifting sequence to facilitate transmitting data and receiving new data substantially simultaneously?

2. Is the Examiner's reason to combine the teachings of these references supported by articulated reasoning with some rational underpinning to justify the Examiner's obviousness conclusion?

FINDINGS OF FACT (FF)

We adopt the Examiner's findings regarding Thomsen and Yasoshima as our own. Ans. 3-10.

ANALYSIS

Based on the record before us, we find no error in the Examiner's obviousness rejection of representative claim 15. We find the Examiner's thorough and cogent reasoning articulated in the Answer (Ans. 6-10) persuasive and adopt it as our own.

Appellant has not persuaded us of error in the Examiner's position that Thomsen's transmitter and receiver FIFO buffers and associated shift register functionality would at least allow transmitting data to the transmitter shift register substantially simultaneously with receiving new data at the receiver shift register. Ans. 7-8. Leaving aside the fact that this capability need only facilitate *substantially* simultaneous data transmission and reception (which is not necessarily simultaneous) as the Examiner indicates (Ans. 9-10), we further note that this limitation merely recites a desired result or capability of the recited shifting sequence, namely *to facilitate* the recited data transmission and reception. In any event, the Examiner's analysis regarding Thomsen's teaching this functionality (Ans. 6-10) is persuasive.

Nor are we persuaded of error in the Examiner's reliance on Yasoshima for teaching integrating Thomsen's multiple FIFOs in a single FIFO (Ans. 7-10), for such an enhancement is nothing more than predictably using prior art elements according to their established functions—an obvious improvement. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). Nor

has Appellant shown that such an enhancement would have been beyond the level of ordinarily skilled artisans. We therefore find the Examiner's reason to combine the teachings of these references supported by articulated reasoning with some rational underpinning to justify the Examiner's obviousness conclusion.

We are therefore not persuaded that the Examiner erred in rejecting representative claim 15 and claims 16, 17, 19, and 20 not separately argued with particularity.

CONCLUSION

The Examiner did not err in rejecting claims 15-17, 19, and 20 under § 103.

ORDER

The Examiner's decision rejecting claims 15-17, 19, and 20 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

peb